REMARKS

This Amendment is responsive to the Office Action dated March 25, 2004. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

At paragraph 2 of the Office Action, the Examiner objected to claims 16 and 17 being duplicates. Claim 17 has been cancelled herein.

At paragraphs 3 through 13 the Examiner rejected claims 1 through 8 and 10 as being anticipated under 35 U.S.C. 102, citing United States patent number 6,625,654 of Wolrich et al. ("Wolrich et al."). Applicants respectfully traverse this rejection.

Wolrich et al. discloses a parallel, hardware-based multithreaded processor. The processor disclosed in Wolrich et al. includes a general purpose processor that coordinates system functions, and a plurality of microengines that support multiple program threads. The Wolrich et al. processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory, and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references. A program thread communication scheme for packet processing is also described in Wolrich et al.

Wolrich et al. further teach that program threads may communicate with a shared resource through a bit set and bit clear mechanism that provides a bit vector. This mechanism of Wolrich et al. allows setting and clearing of individual bits and performing a test and set on individual bits to control a shared resource. The bit vector used in Wolrich et al. signals the non-emptiness of output queues. When a receive program thread enqueues a packet, the receive

scheduler of Wolrich et al. sets a bit, and the transmit scheduler can examine the bit vector to determine the state all queues.

Nowhere in Wolrich et al. is there disclosed or suggested any method or system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> providing a processor including a plurality of analysis machines and a plurality of computer resources, ***wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines***;
> executing each instruction thread in one of the plurality of analysis machines; and
> sharing services of at least one of the plurality of computer resources between at least two of the plurality of analysis machines during the execution of each instruction thread (emphasis added)

as in the present independent claim 1. Analogous features are also present in the present independent claim 5. In contrast, Wolrich et al. draw a distinction between parallel processing and pipeline processing. Specifically, in the Background section, Wolrich et al. state as follows:

> Parallel processing demands concurrent execution of many programs in a computer, in contrast to sequential processing. In the context of a parallel processor, parallelism involves doing more than one thing at the same time. ***Unlike a serial paradigm where all tasks are performed sequentially at a single station or a pipelined machine where tasks are performed at specialized stations, with parallel processing, a plurality of stations are provided with each capable of performing all tasks.*** That is, in general all or a plurality of the stations work simultaneously and independently on the same or common elements of a problem. Certain problems are suitable for solution by applying parallel processing. (emphasis added)

Thus the teachings of Wolrich et al. are directed towards alternatives to "a pipelined machine where tasks are performed at specialized stations". Accordingly, Wolrich et al. include no hint or suggestion of any system or method including multiple analysis machines, each of

which includes *an internal pipeline and is communicably coupled to a plurality of shared pipelines,* as in the present independent claims 1 and 5.

For the above reasons, Applicants respectfully urge that Wolrich et al. does not disclose or suggest all the features of the present invention as set forth in independent claims 1 and 5. Accordingly, Wolrich et al. does not anticipate the present independent claims 1 and 5 under 35 U.S.C. 102. As to dependent claims 2-4, 6-8, and 10, they each depend from independent claims 1 and 5, and are respectfully believed to be patentable over Wolrich et al. for at least the same reasons.

At paragraphs 14-24 of the Office Action, the Examiner rejected claims 9 and 11-18 for obviousness under 35 U.S.C. 103, again citing Wolrich et al., and additionally citing United States patent number 6,081,860 of Bridges et al. ("Bridges et al."). Applicants respectfully traverse this rejection.

Bridges et al. disclose a process and system for transferring data including a slave device connected to a master device through an arbiter device. The master and slave devices of Bridges et al. are connected by a single address bus, a write data bus and a read data bus. The arbiter device of Bridges et al. receives requests for data transfers from the master devices and selectively transmits the requests to the slave devices. The master devices and the slave devices in the Bridges et al. system are further connected by a plurality of transfer qualifier signals which may specify predetermined characteristics of the requested data transfers. Control signals are also communicated between the arbiter device and the slave devices of Bridges et al. to allow appropriate slave devices to latch addresses of requested second transfers during the pendency of current or primary data transfers so as to obviate an address transfer latency typically required for the second transfer. The design of the Bridges et al. system is configured to advantageously

function in mixed systems which may include address-pipelining and non-address-pipelining slave devices. The relevant teachings of Wolrich et al. are discussed above with regard to the rejections in paragraphs 3-13 of the Office Action.

Nowhere in Wolrich et al. is there disclosed or suggested any system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> ***a plurality of analysis machines to execute a plurality of instruction threads, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines***;
>
> a plurality of computer resources operationally connected to said plurality of analysis machines;
>
> wherein each instruction thread executes in one of said plurality of analysis machines, and services of at least one of said plurality of computer resources are shared between at least two of said plurality of analysis machines during the execution of each instruction thread. (emphasis added)

as in the present independent claim 5, from which dependent claims 9 and 11-18 depend. As noted above, Wolrich et al. teaches a system for parallel processing that is an alternative to a pipelined machine. Bridges et al. describe a technique for enhancing a processor local bus to allow for address pipelining, but provide no hint or suggestion of any method or system for providing analysis machines each including an internal pipeline and being communicably coupled to a plurality of shared pipelines, as in the present independent claim 5. Thus the combination of Wolrich et al. and Bridges et al. provides no teaching of significant features of the present independent claim 5, particularly with regard to *the structure of the claimed analysis machines with regard to the internal pipeline*, and with regard to *the structure of the claimed analysis machines with regard to the plurality of shared pipelines*.

For the above reasons, Applicants respectfully urge that the combination of Wolrich et al. and Bridges et al. fails to disclose or suggest all the features of the present independent claim 5, from which claims 9 and 11-18 depend. Accordingly, the combination of Wolrich et al. and Bridges et al. does not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to the present independent claim 5, and/or dependent claims 9 and 11-18. Dependent claims 9 and 11-18 would therefore not be obvious to one skilled in the art. Reconsideration of all pending claims is respectfully requested.

For these reasons, and in view of the above amendments, Applicants respectfully request that all rejections and objections be withdrawn. The application is now considered to be in condition for allowance, and such action is earnestly solicited.

Applicants have made a diligent effort to place the application in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

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Date

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